FT-UNSHADES: a new system for SEU injection, analysis and diagnostics over post synthesis netlists

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Summary

- Brief Description of FT-UNSHADES project
  - What is not FT-UNSHADES?
- FT-UNSHADES secret: Partial Reconfiguration
- The system
  - Design flow
  - Tests procedure
  - Analysis procedure
- Benchmarking
- Conclusions
- The Future
- Q&A

Brief Description of FT-UNSHADES project

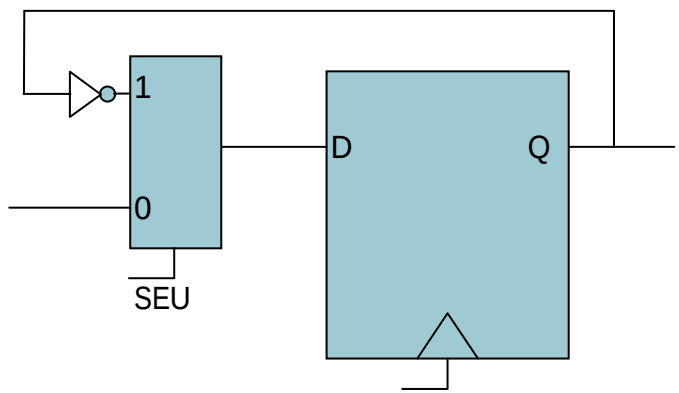
Radiation environment emulator

Use a huge FPGA from Xilinx

Initial objective: Provide a test and analysis framework to check the design protections (TMRs and voters, EDACs, ...) of an IP or ASIC, **BEFORE** place and route and fabrication

Current solutions:

- VHDL simulators
- Instrumenting FFs



What FT-UNSHADES isn't?

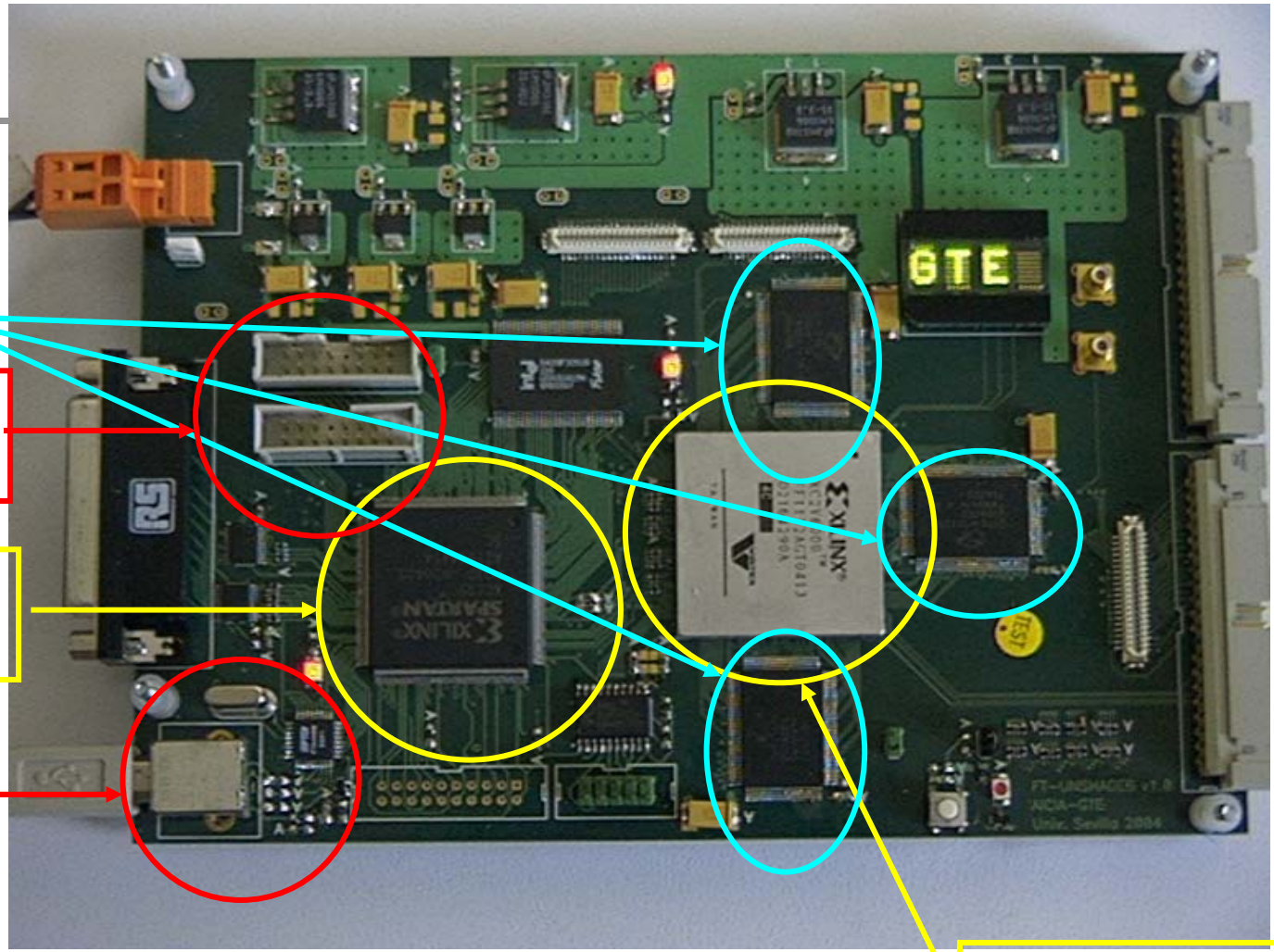
- It's not a platform for radiation testing of FPGAs
- It's not designed for being inserted into a radiation environment

FT-UNSHADES secret: Xlinx partial reconfiguration

- Takes advantage of partial reconfiguration techniques for fault injection and capture and readback for design observation
- Changes in FF state are made from the configuration circuit. No manipulation is needed previous to synthesis.
- Direct manipulation of bitstream slices speeds-up the bit-flip induction.
- Large circuits with huge stimulus vector database are tested at hardware speed

CIRCUIT IS TREATED AS A *BLACK BOX*

System elements: the board



Vector Memories 2Mx102

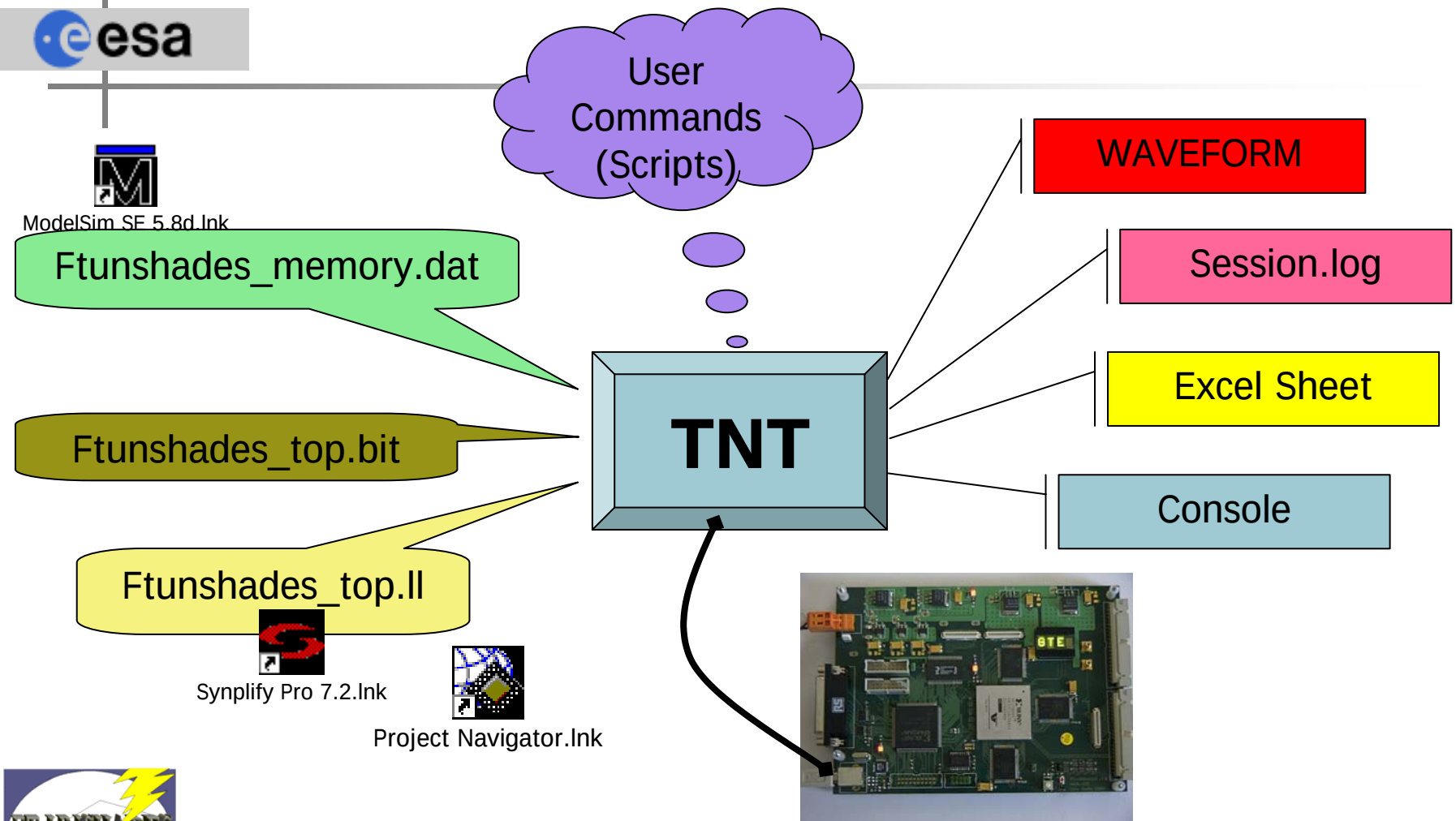
Multi Board Link

Control FPGA Spartan II-50

PC-Host USB Link

SYSTEM FPGA Virtex II

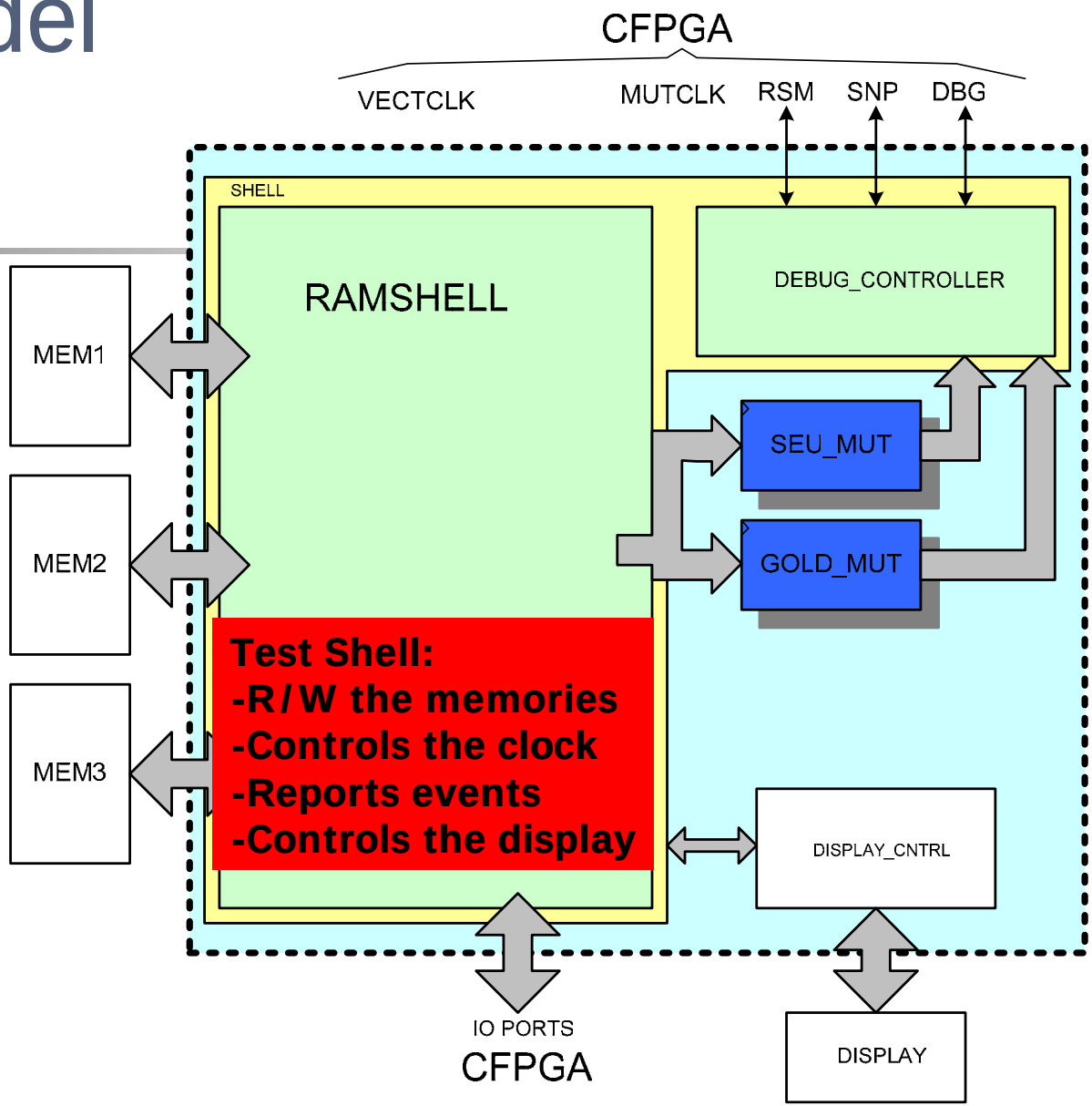
System elements: the software



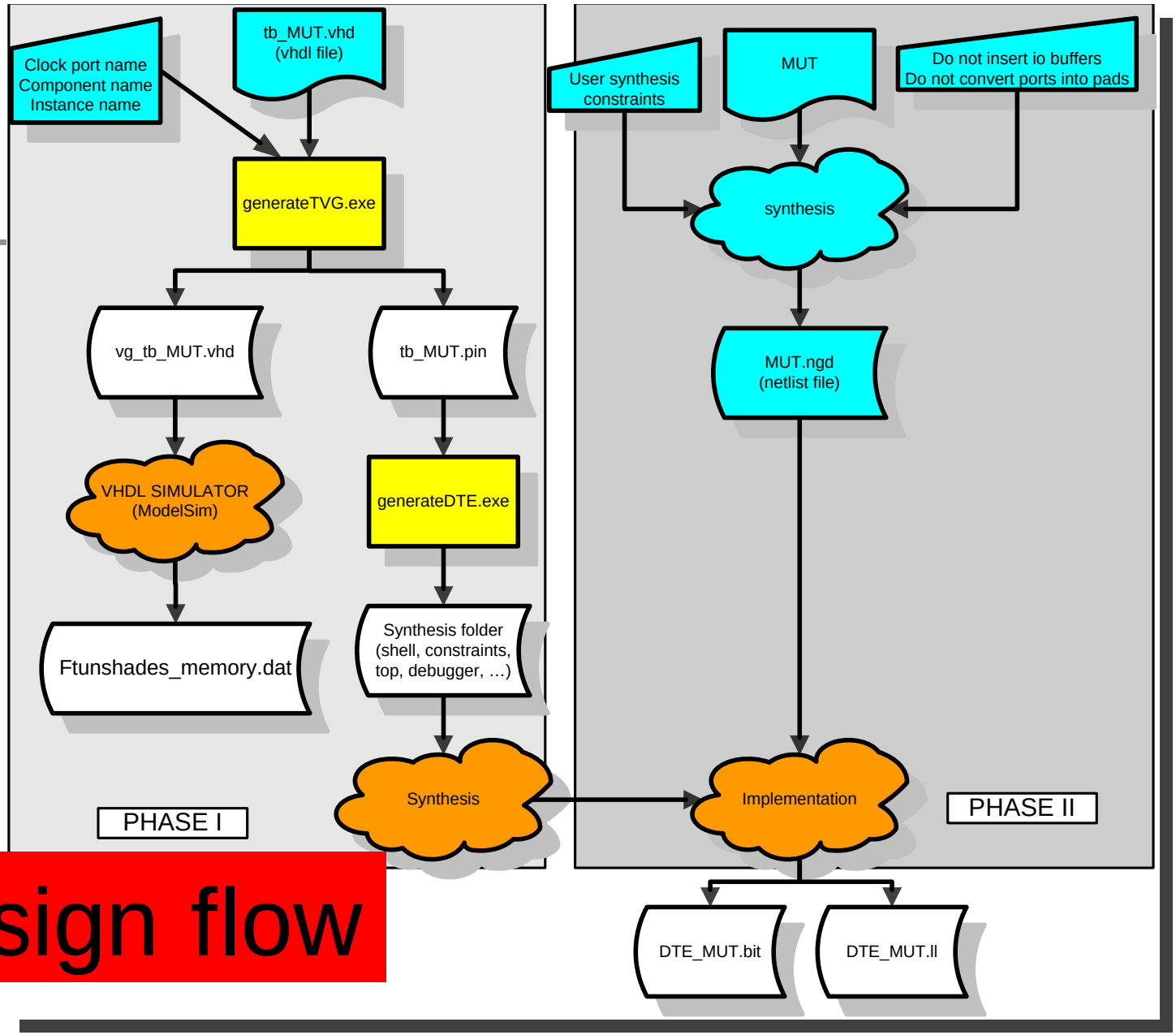
Test Model

Two identical instances of the Module Under Test are synthesised with the Test Shell:
-SEU_MUT receives the bit flips
-GOLD_MUT allows comparisons

Both MUTs must be treated as Macros, to avoid their synthesis collapsing.



Design flow


Clock port name
Component name
Instance name
tb_MUT.vhd
(vhdl file)
generateTVG.exe
vg_tb_MUT.vhd
tb_MUT.pin
VHDL SIMULATOR
(ModelSim)
generateDTE.exe
Ftunshades_memory.dat
Synthesis folder
(shell, constraints,
top, debugger, …)
Synthesis
PHASE I
User synthesis
constraints
MUT
Do not insert io buffers
Do not convert ports into pads
synthesis
MUT.ngd
(netlist file)
Implementation
PHASE II
DTE_MUT.bit
DTE_MUT.ll

Test Procedure: When, Where and How

1. Configure the System FPGA and download the input vector database
2. Specify the test level (How):
   1. Damage
   2. Output
   3. Latent
3. Specify time (When)
4. Specify location (Where)
5. Specify method and conditions (How)
6. RUNTEST <- Fault Dictionary is generated

A single test process:

SEU(T,L)

A single test run has the following schedule:

1. Program the time counter with T
2. Give Module Reset
3. Launch the system to stop at T
4. Get frames related to L
5. Induce SEU at L
6. Resume system
7. Watch events to check SEU effects.

Analysis Procedure:

- *Step*: Run a single clock cycle and check internal evolutions
- *AnRun* Command: Run the emulation to the insertion point. Then analyse.
- *Diff* command: Compare the states of Gold/SEU instances to check internal propagation

Benchmarking

	MUT								DTE					
Name	Sint.	Inputs/Bidir	Clock Cycles	Slices	FFs	Max Delay	Eq. Gates	Wrap	Synth	Slices	FFs	Max Delay	Eq. Gates	Clk Freq
EDAC 8 Cycle	Synplify	25 / 0	38106000	108	40	11,917 ns	6678	Y	XST	1417	919	8,93	292892	87,982
EDAC 16 Humming	Synplify	41 / 0	4400000	38	60	7,37 ns	909	Y	XST	1337	1132	9,775	350089	85,793
CTM	Synplify	73 / 0	112649	1025	753	9,426 ns	16237	Y	XST	3668	2675	9,155	446836	49,796
CAN Core	Synplify	93 / 0	419231	373	371	7,83 ns	7116	Y	XST	2455	1950	9,2	429127	47,495
CAN AMBA	Synplify	69 / 0	26500	764	753	13,718 ns	12726	Y	XST	3255	2556	9,995	439854	42,384
CORDIC	XST	51 / 0	200000	282	192	9,041 ns	6839	Y	XST	1677	1317	9.845	93314	84,868
CORDIC-XTMR	XST	51 / 0	200000	1172	796	9,31 ns	28057	Y	XST	4228	2798	9,97	350803	71,882
CTM-TMR	Synplify	86 / 0	26410	6572	2352	21,496 ns	92844	Y	XST	14744	6264	16,27	547000	62,452
CUC	Synplfy	18 / 0	25000	255	138		4753	Y	XST	1529	1194	9,702	289507	47,143

DATA	Test Runs	Time (secs)	Comments	Comments to behaviour
EDAC 8 Cycle	100	467,44	A register has been inserted at the input for SEU insertion	All SEUs seen after one clock cycles
EDAC 16 Humming	1000	146,45	A register has been inserted at the input for SEU insertion	All SEUs seen after one clock cycles
CTM	1000	202,71	ESA	
CAN Core	1000	268,96	ESA	No SEUs seen at the output
CAN AMBA	1000	148,59	ESA	No SEUs seen at the output
CORDIC	1000	138,23	A fully pipelined CORDIC	All SEUs seen after few clock cycles
CORDIC-XTMR	1000	139,27	A fully pipelined CORDIC with Xilinx TMR	Double SEU fail: 5%
CTM-TMR	1000	144,21	ESA TMR	Fully Double SEU protected
CUC	1000	144,32	ESA	

Conclusions

- Circuit Overhead: 100.000 system gates
- Fault injection time: 1,4ms (XC2V6000) and 1,6ms (XC2V8000)

- A tool for TMR verification
- Analysis
- If you want to reduce the protection level ... or optimize critical areas

Future of FT-UNSHADES

- Large circuit benchmarking (Leon2)
- Output files for automatic TMR insertion tools, in order to produce selective protection
- Layout restrictions for multi SEUs

Thank you for your attention

Q&A

http://www.gte.us.es/~aguirre/Web_unshades/ftunshades.htm