FT-UNSHADES

Microelectronic Presentation Day
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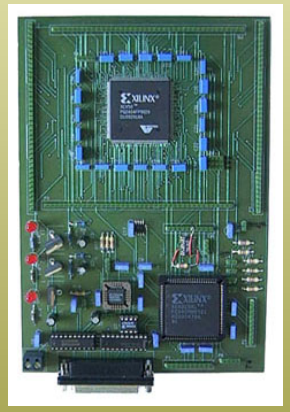
FT-UNSHADES credits

- UNiversity of Sevilla HArdware DEbugging System.
  - Involved since 1996 in projects related to FPGA technology
  - Wide experience in VLSI and FPGA design
  - Software developers and hardware designers
  - UNSHADES-1 and UNSHADES-2

  http://www.gte.us.es/~aguirre/Web_unshades/index



FT-UNSHADES. The Problem

- Provide to VLSI Designers a feedback of the reliability of a module against SEUs during design phase
- Provide a toolbox for deep analysis when a weak area is found.
- SEU immunity tests performed in a reasonable period of time

Current Approaches

- HARDWARE approaches
  - Radiation Chamber. (Expensive, Poor analysis, Chip fab is required)
  - FPGA Prototype (till today): (Circuit overhead, SEU injection through external pins, poor analysis, many synthesis cycles and VHDL manipulation)
- SOFTWARE approaches
  - VHDL simulator (SLOW, Usually needs netlist changes)

Current approaches (I)

Radiation Chamber

- Run Time Test

- Non Intrusive

- Deep Analysis

- Costs

Current approaches (II)

FPGA Emulators

- Run Time Test

- Non Intrusive

- Deep Analysis

- Costs

Current approaches (III)

HDL Simulators

- Run Time Test

- Non Intrusive

- Deep Analysis

- Costs

FT-UNSHADES

FT-UNSHADES System

- Run Time Test

- Non Intrusive

- Deep Analysis

- Costs

FT-UNSHADES. What's new?

- Use Xilinx FPGA technology for circuit emulation
- Use configuration ports with partial readings and writings of configuration frames, speeds up SEU injection
- Fully automatic test, even for submodules

FT-UNSHADES. Know how

The key of the problem is to modify a FF state during run-time (SEU) using a non intrusive method

without extra circuitry= zero overhead

UNIVERSITY of Sevilla Proprietary Patents:

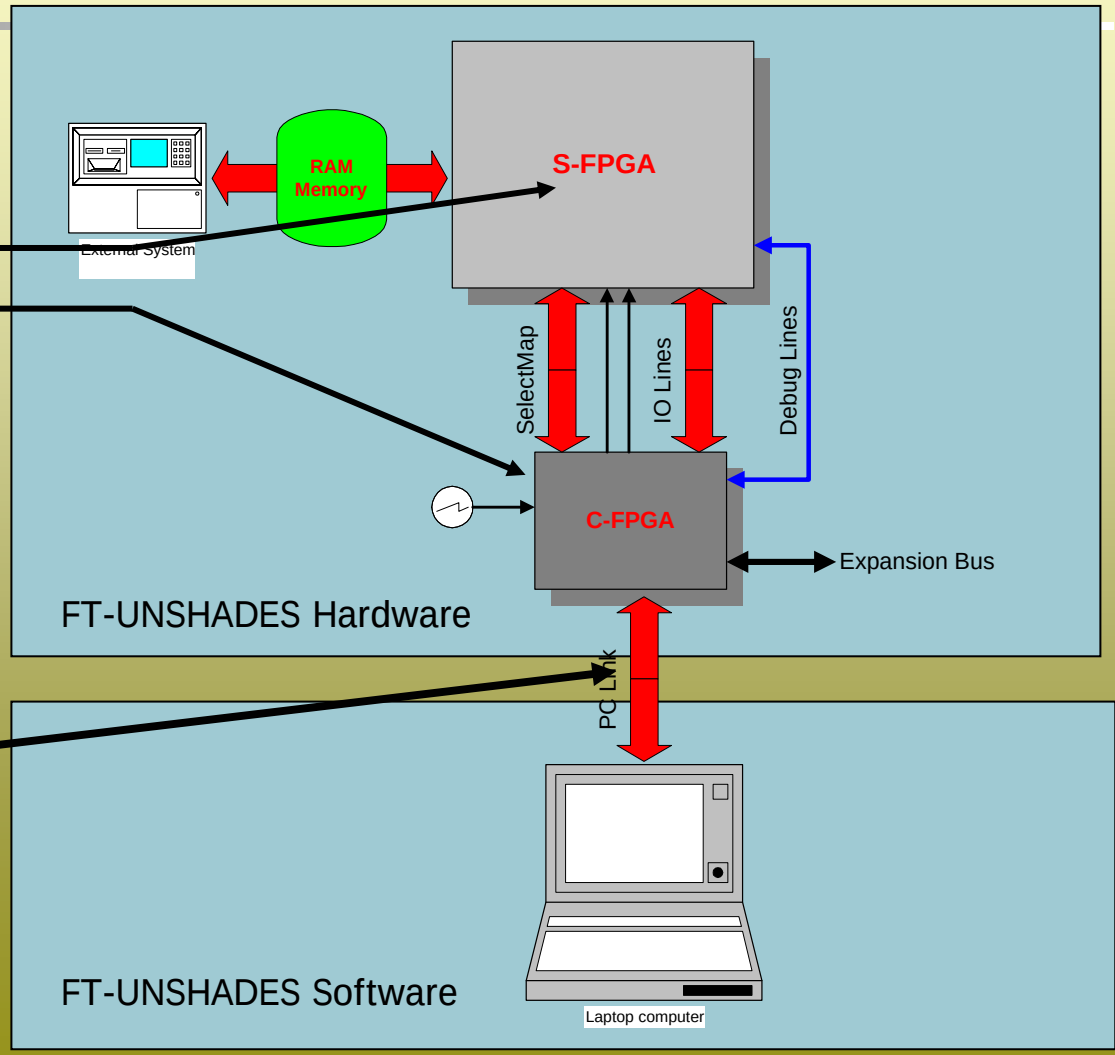
- **"Method for the functional test of large digital circuits using hardware emulators". W ES-02/00571**

- **"Procedure for the induction of register values in an emulated circuit using integrated hardware emulation"**
  Patent Pending P200203051

FT-UNSHADES System

Two FPGA's
- **System FPGA (S-FPGA)**
- **Control FPGA (C-FPGA)**

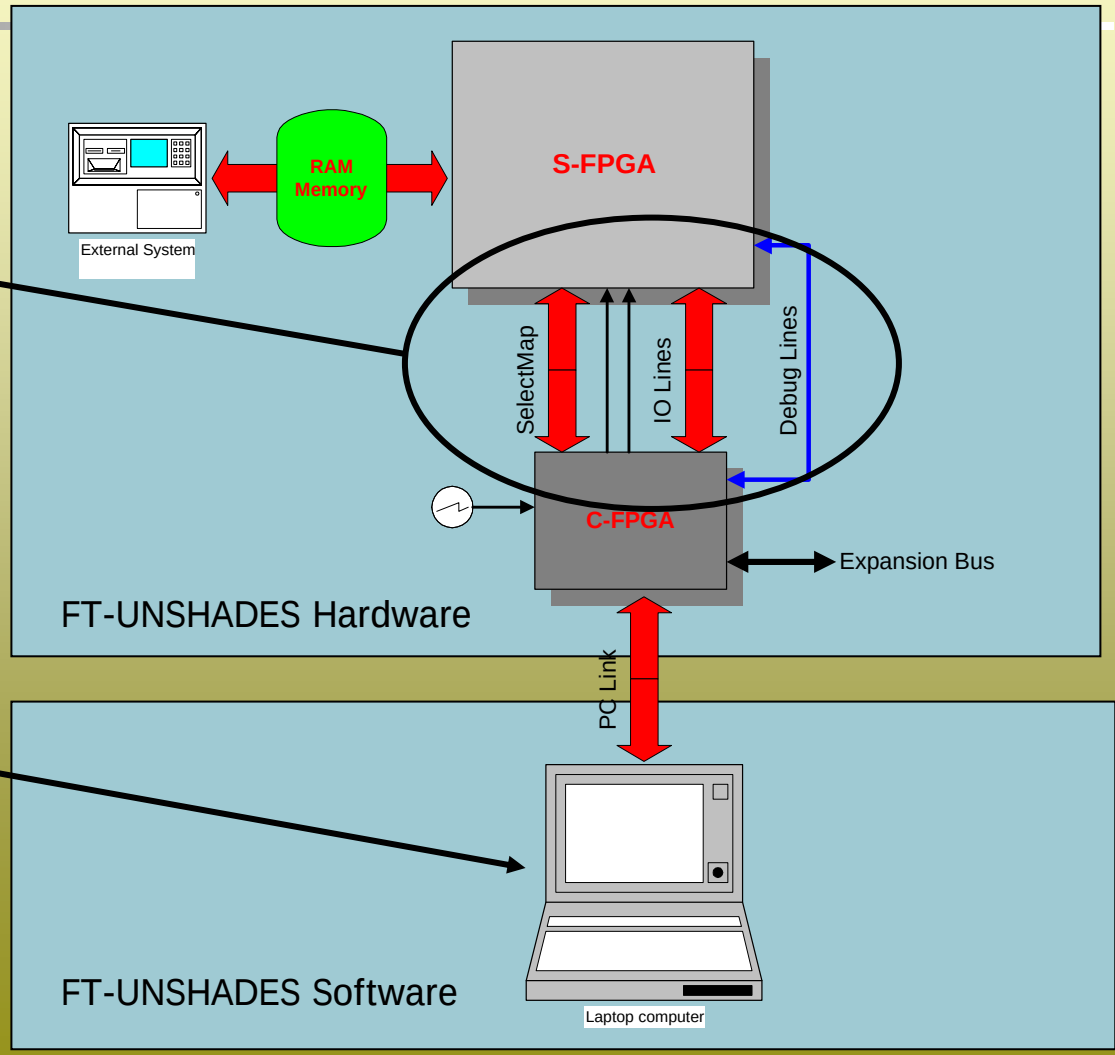
Communication:
- **1.5MB/s (USB / EPP)**
- **Multi-Board**



FT-UNSHADES System

Links:
- **Configuration**
- **Clock Generation**
- **Special debug Lines**
- **General Purpose I/O**

Software:
- **Board handling**
- **Test Definition**
- **Analysis**



FT-UNSHADES. Handling vectors

RTL netlist

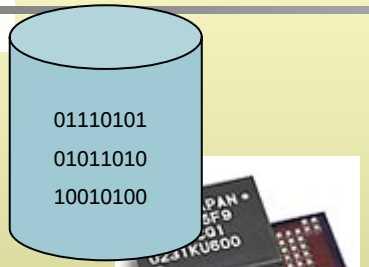
Test Bench

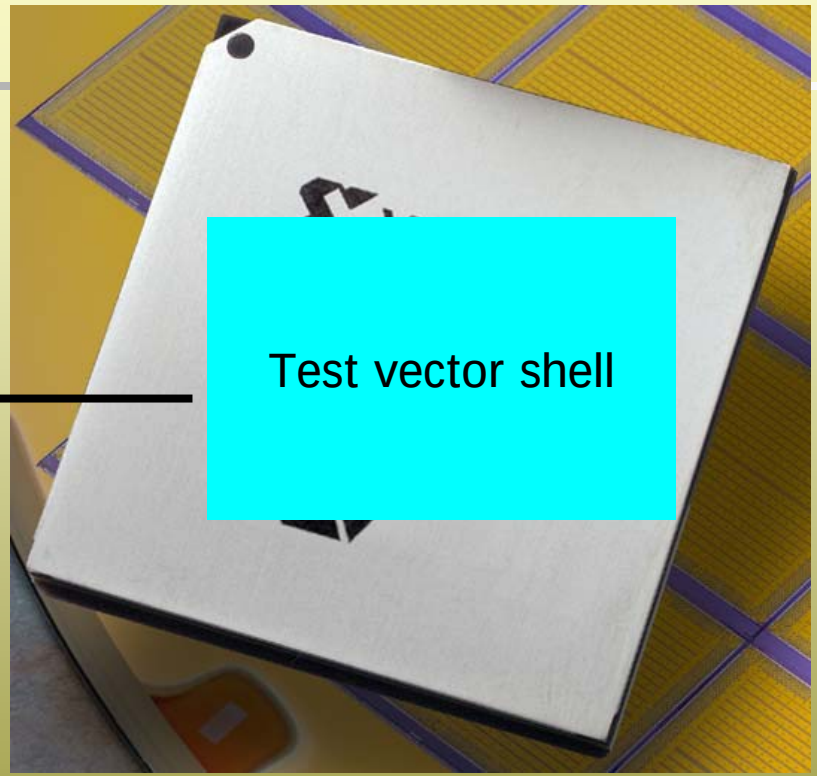
A	B(0)	B(1)	B(2)	C	D
0	1	1	1	0	0
1	0	0	1	0	0
0	0	0	1	1	0
1	0	1	1	1	1
0	1	1	0	0	0

01110101
01011010
10010100

User testbed is used to create test vectors

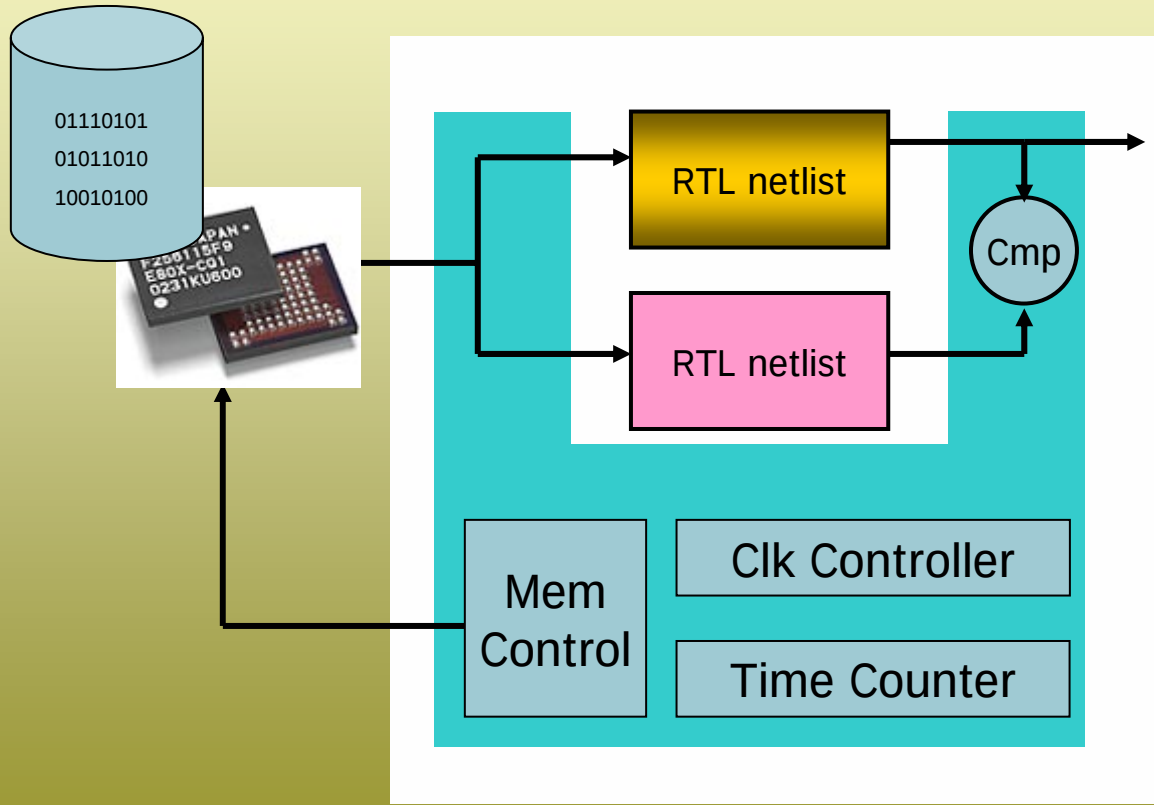
FT-UNSHADES. Handling vectors





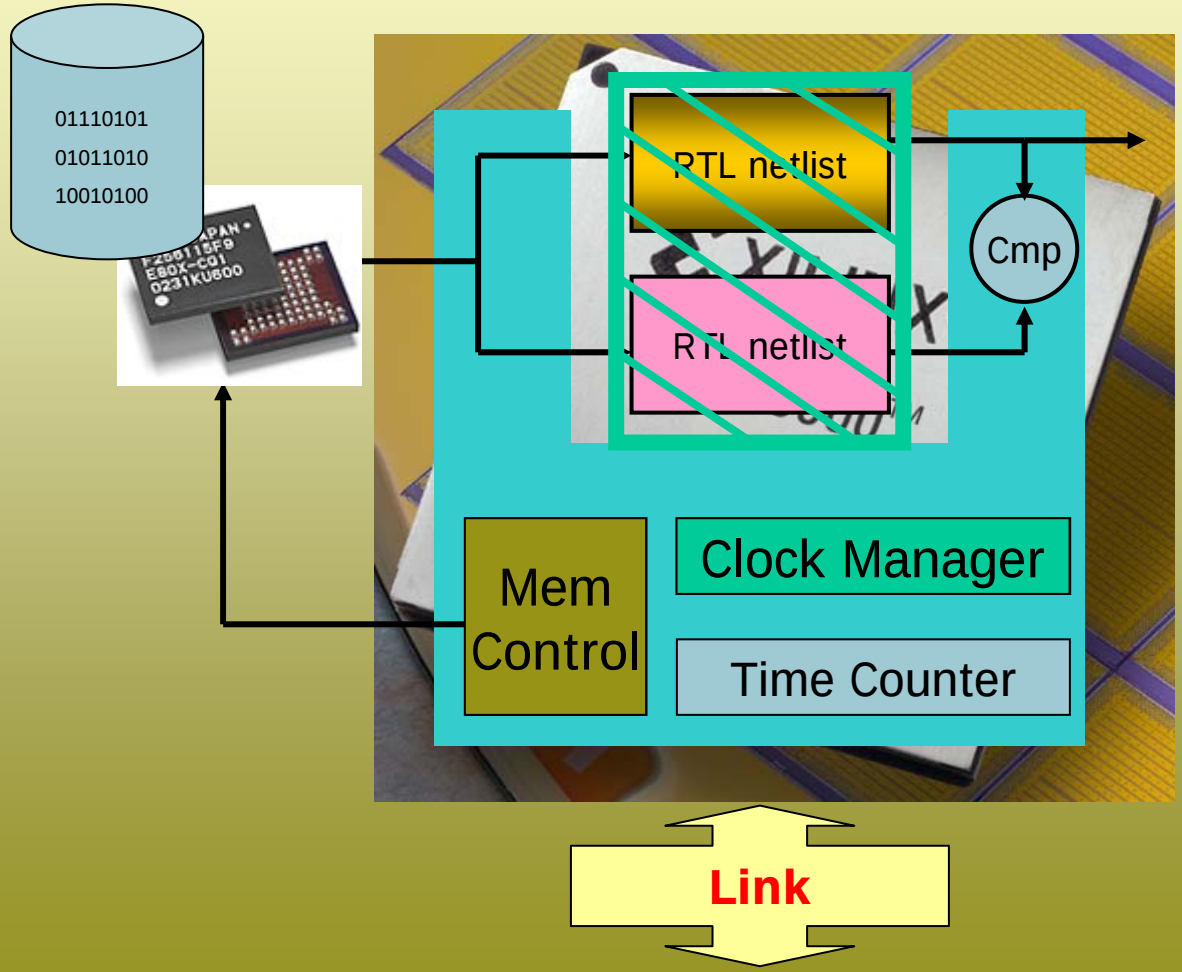
Vectors are stored in on-board memories

FT-UNSHADES. System FPGA



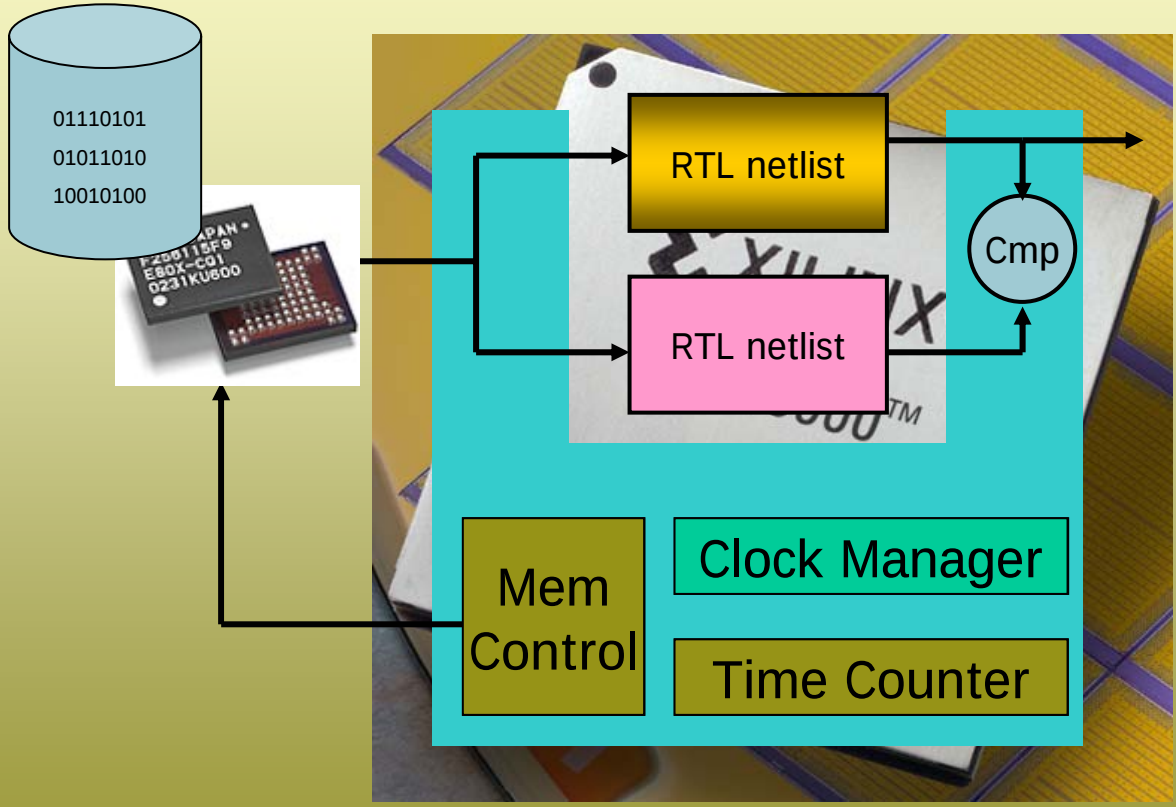
Two copies of the design are instanced within a test shell

FT-UNSHADES. System FPGA



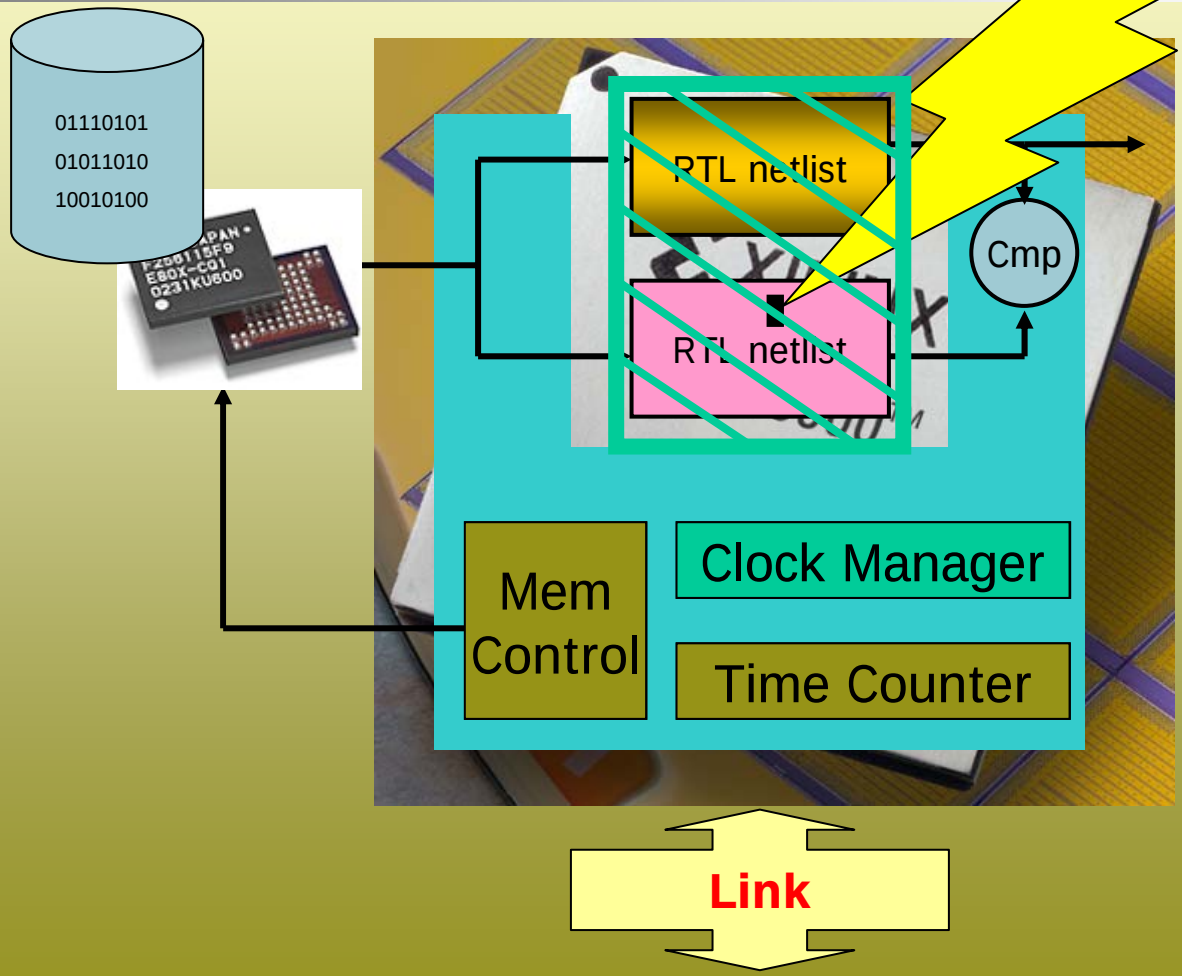
Design is frozen and SEU insertion cycle programmed

FT-UNSHADES. System FPGA



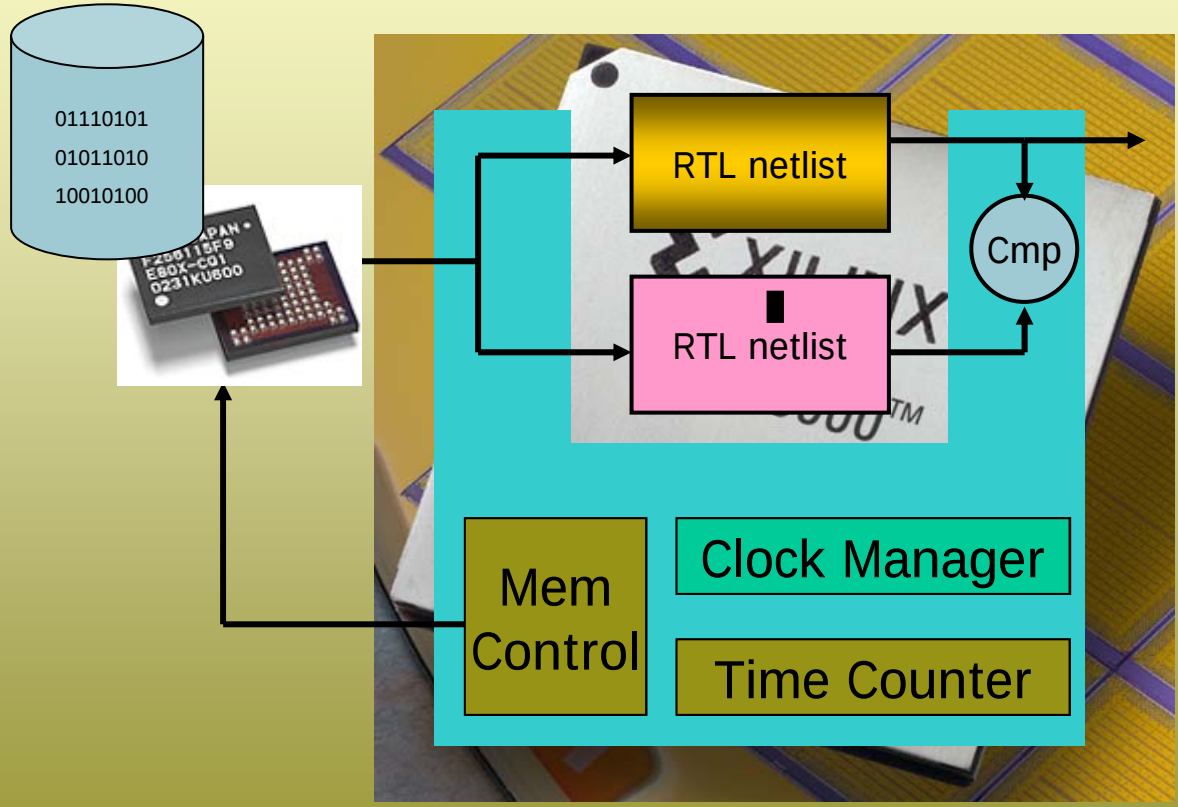
Vectors are applied at system speed until SEU cycle is reached

FT-UNSHADES. Syste FPGA



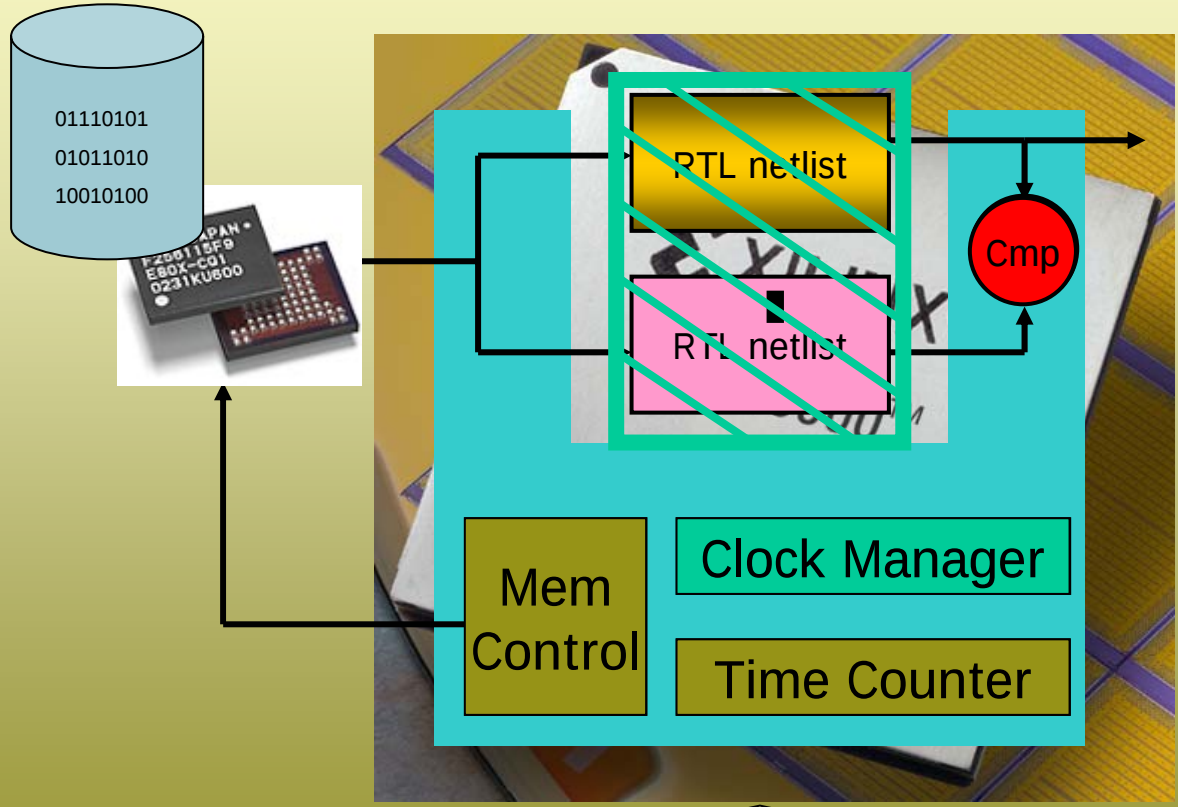
Selected flip-flop has SEU inserted

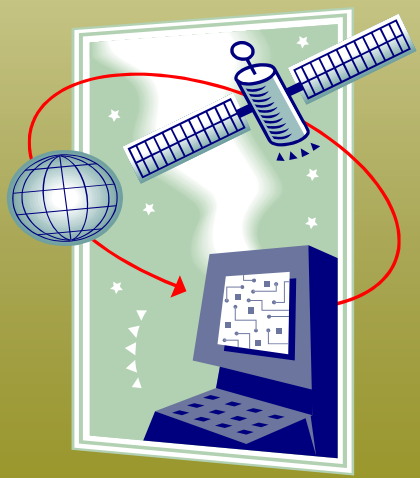
FT-UNSHADES. System FPGA



Design advances again at system speed

FT-UNSHADES. System FPGA





Link

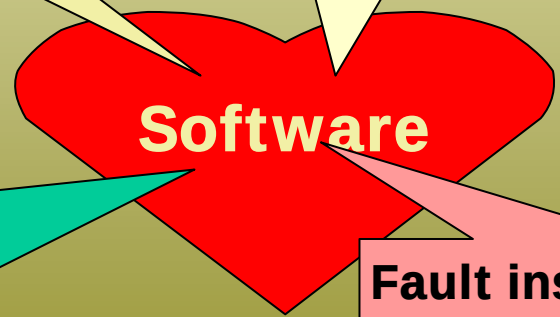
If SEU produces and error output and cycle error are recorded

FT-UNSHADES. Software

Test Vectors Services:
- **Format test vectors**
- **Transfer vectors to board**

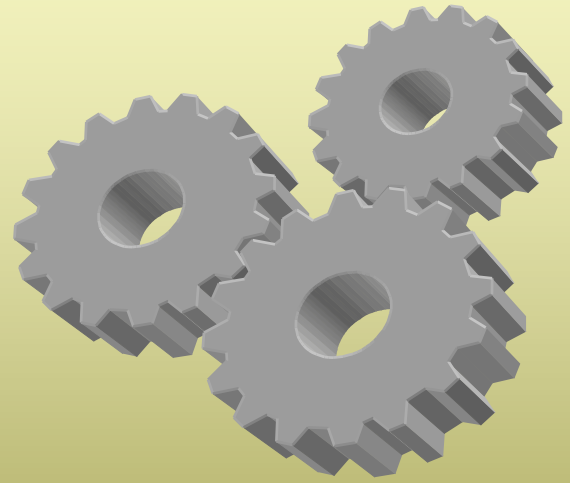
Board Services:
- **Configure SFPGA**
- **Program CLOCK rate**
- **Handle Communications**

Fault testing:
- **Handle Time counter (WHEN)**
- **Handle Flip-Flop Placement (WHERE)**
- **Define Injection Strategies (HOW)**



Fault insertion analysis:
- **Store faults**
- **Classify faults (Damage, Latent,...)**
- **Single Stepping Analysis**

FT-UNSHADES Software



- C++ Based Code
- Console Mode
  - Wild Cards
  - Script self-generation
  - User defined macro-commands
- Adapted to Xilinx Design Flow
- Fully automatic test flow

Using FT-UNSHADES

1. RTL netlist of a module or circuit described in VHDL or Verilog
2. Use your Test Bench to build functional vectors file
3. RUN Test vector handling services
4. Synthesise netlist with the test shell using ISE
5. Define fault injection strategy
6. RUN FT-UNSHADES campaign and wait for your fault dictionary



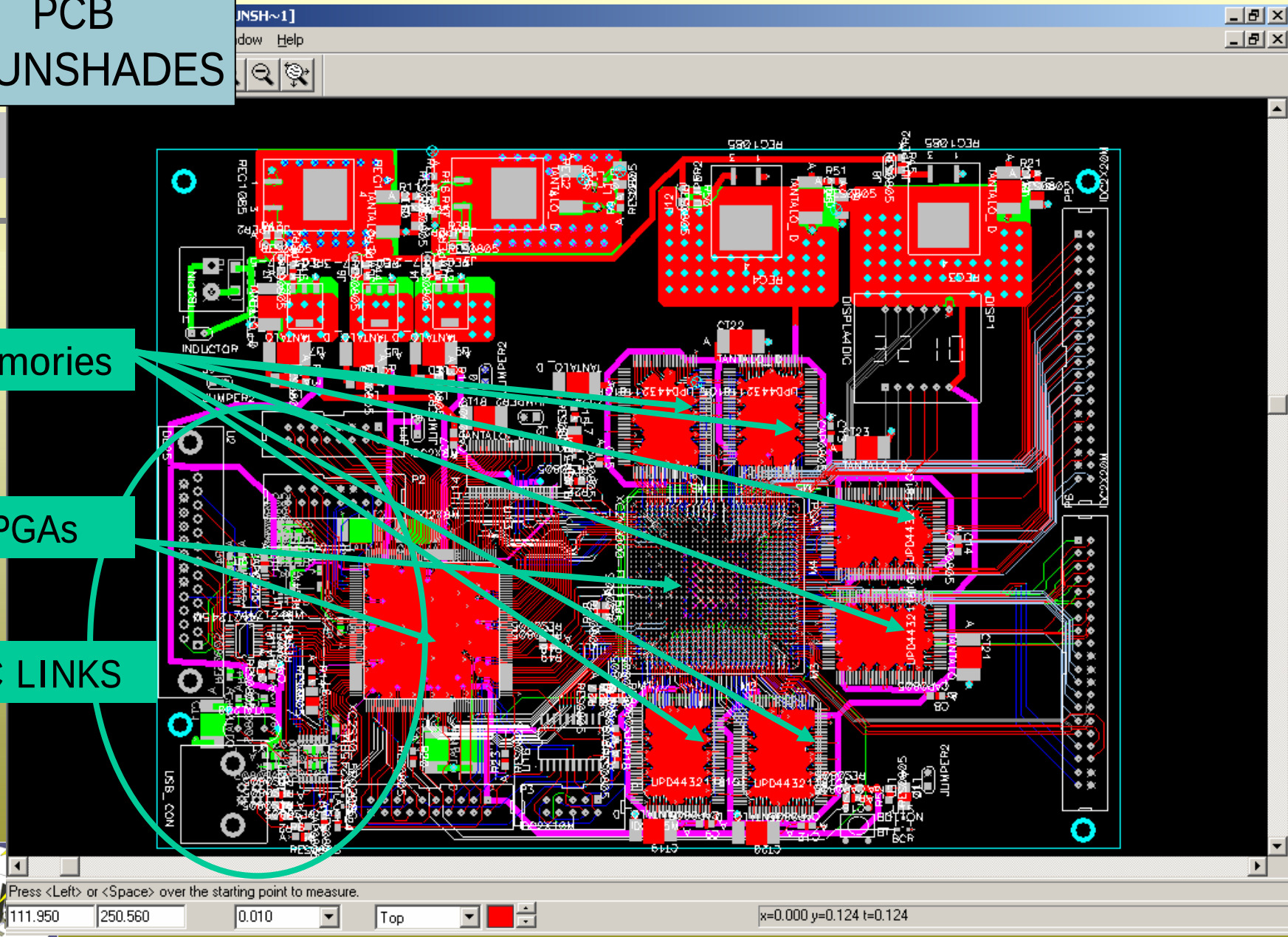


Fault dictionary

- Injection vector: 400.000
- Fault Place:
  /toptest/mutfaulty/registerfile/reg(5)
- SEU Toggle: 1☛0
- IO fault vector: 400.027
- IO mismatched: addr(3) <-Damage

This information is enough for a post campaign analysis. FT-UNSHADES can produce single stepping analysis and provide the internal state information for a waveform viewer

PCB FT-UNSHADES



Technical specifications

- SFPGA: XC2V6000-FF1152 (6M gates)
- Maximum board clock speed 160MHz
- Vector memory: 6 units of 2M words x 16bits
- Memory clock speed: 100MHz (200Mhz units could be mounted)
- PC-Link: EPP 1.9 or USB 2.0

Expected performance (medium)

- Assume:
  - Design speed: 50MHz
  - Memory Speed: 100MHz
  - Link Speed: ~1.5MB/s
  - Vectors: 2Mb
  - Bytes per frame 7872/8=984
- Testing time: 2M cycles / 50MHz=40ms
- PC accessing time: 6 x 984 /1,5MHz=4ms

Size independant!!!

One fault in injected every 44ms~80.000 faults/hour

Optimistic: 25ms~144000 faults/hour

Pessimistic: 100ms~36000 faults/hour

FT-UNSHADES. Conclusions

- New design for reliability platform
- Easy to use. Full automatic design flow.
- Analysis toolbox
- References:

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FT-UNSHADES completion is scheduled for September 2004